Printed Page:- 03 Subject Code:- ACSAI0302

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - THEORY EXAMINATION (2023 - 2024)

Subject: Logic Design and Computer Architecture

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. The operation of insertion in stack is called _____. (CO1) 1

(a) POP

(b) PUSH

(c) Evaluation Create

(d) None

1-b. The ALU makes use of _____ to store the intermediate results. (CO1) 1

(a) Accumulator

(b) Program Counter

(c) Stack Pointer

(d) Address Register

1-c. IEEE stands for _____ . (CO2) 1

(a) Instantaneous Election Electrical Engineering

(b) Institute of Emerging Electrical Engineers

(c) Institute of Emerging Electronic Engineers

(d) Institute of Electrical and Electronics engineers

1-d. Carry lookahead adder uses the concepts of _____. (CO2) 1

(a) Inverting the inputs

(b) Complementing the outputs

(c) Generating and propagating carries

(d) None of the mentioned

1-e. How many address bits are required to represent a 32 K memory? (CO3) 1

(a) 10 bits
(b) 12 bits
(c) 14 bits
(d) 15 bits

1-f. Two important fields of an instruction are _____ & _____.(CO3) 1

(a) Opcode
(b) Operand
(c) mode
(d) Both 1 & 2

1-g. Time for replacing the block from memory, is referred as _____. (CO4) 1

(a) miss penalty
(b) Penalty
(c) Hit
(d) Miss

1-h. Maximum time required before a dynamic RAM must be refreshed is _____. (CO4) 1

(a) 2 ms
(b) 4 ms
(c) 6 ms
(d) 8 ms

1-i. The transmission on the asynchronous bus is also called as _____ mode transmission. (CO5) 1

(a) Pulse
(b) Switch
(c) Signal
(d) None of the mentioned

1-j. MAR stands for _____.CO5 1

(a) Main address register
(b) Memory address register
(c) Main accessible register
(d) Memory accessible register

2. Attempt all parts:-

2.a. What are the functions of ALU and Control Unit? (CO1) 2

2.b. Define the concept of Half adder. (CO2) 2

2.c. What is meant by instruction? (CO3) 2

2.d. What is SRAM and DRAM? (CO4) 2

2.e.	Explain different types of peripheral devices?(CO5)	2
SECTION-B		30
3. Answer any five of the following:-		
3-a.	Draw the diagram of bus system that uses three state buffers and 2:4 decoder instead of multiplexers and Explain how it works. (CO1)	6
3-b.	Show the block diagram of the hardware that implements the following register transfer statement: P: R2 <----- R1. (CO1)	6
3-c.	Sketch the flow diagram of division algorithm with suitable example. (CO2)	6
3-d.	Explain IEEE standard for Floating Point Numbers.(C02)	6
3.e.	Explain the concept of hardwired with the help of suitable example. (CO3)	6
3.f.	List the difference between following - a) RAM and ROM b) Static RAM and Dynamic RAM. (CO4)	6
3.g.	Write the difference between serial and parallel communication.(CO5)	6
SECTION-C		50
4. Answer any one of the following:-		
4-a.	Explain push and pop operations of Register stack and Memory stack. (CO1)	10
4-b.	What is register? Explain General Register organization with control word. (CO1)	10
5. Answer any one of the following:-		
5-a.	Explain the working of 4 bit Carry Look Ahead Adder with help of example. (CO2)	10
5-b.	Calculate 5 X 6 with the help of signed magnitude algorithm. (CO2)	10
6. Answer any one of the following:-		
6-a.	Differentiate between programming and microprogramming using suitable examples. (CO3)	10
6-b.	What is pipelining? Explain the difference between arithmetic and instruction pipeline. (CO3)	10
7. Answer any one of the following:-		
7-a.	What is Memory hierarchy? Explain the purpose to construct such memory hierarchy in digital computers. (CO4)	10
7-b.	Define set associative cache mapping using suitable example. (CO4)	10
8. Answer any one of the following:-		
8-a.	Draw the block diagram of DMA controller. (CO5)	10
8-b.	What is Interrupt? Explain the different types of Interrupts. (CO5)	10